REMARKS

Claims 1, 5, 11, 13, 17 and 24 have been amended. Claims 1-25 and 44-59 remain in the application. Reconsideration of the application in view of the amendments and the remarks to follow is requested.

The title is amended.

Claims 1, 2, 5-21, 24, 25 and 44-49 stand rejected under 35 U.S.C. §102(b) as being anticipated by Brown (5,418,180). Claims 50-57 stand rejected under 35 U.S.C. §102(3) as being anticipated by Wu et al. (5,913,129). Claims 3, 4, 22 and 23 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Brown in view of Kim et al. (5,324,679). Claims 58 and 59 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Wu et al. in view of Kim et al. Claims 50-59 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 44-51 of U.S. Patent No. 6,207,523.

Regarding the anticipation rejection against claim 1 based on Brown, such claim is amended to recite forming a solid mass of silicon material within an opening formed over a doped region of a silicon substrate, the mass comprising **only** two forms of silicon. No new matter is added as the originally-filed application supports the amendment language at, for example, Figs. 7-13. Brown teaches an amorphous silicon 61 formed of three silicon layers 31, 41, and 51 (Figs 2-8). In no fair or reasonable interpretation does Brown teach or suggest a mass of silicon material comprising **only** two forms of silicon as recited in

claim 1. Consequently, Brown, singularly or in any combination with the art of record, fails to teach or suggest a positively recited limitation of claim 1, and therefore, claim 1 is allowable. Applicant respectfully requests allowance of claim 1 in the next office action.

Claims 2-3 and 44 depend from independent claim 1, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the anticipation rejection against claim 5 based on Brown, such claim is amended to recite forming a solid mass of silicon material over a doped **diffusion** region of a silicon substrate, the mass comprising exposed doped silicon and exposed undoped silicon, and including undoped silicon in contact with the doped **diffusion** region. No new matter is added as the originally-filed application supports the amendment language at, for example, Figs. 8-13. Brown teaches three layers of silicon form a capacitor storage node over a diffusion region 11, and one of the three layers, a doped silicon layer 41, is in contact with the diffusion region 11 formed in substrate 10 (col. 5, lns. 15-22; Fig. 7b). Accordingly, it is inconceivable that a doped silicon layer 41 in contact with the diffusion region 11 as taught by Brown could teach or suggest undoped silicon in contact with the doped **diffusion** region as recited in claim 5. Brown, singularly or in any combination of the art of record, fails to teach or suggest

a positively recited limitation of claim 5, and therefore, claim 5 is allowable. Applicant respectfully requests allowance of claim 5 in the next office action.

Claims 6-10 and 45 depend from independent claim 5, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the anticipation rejection against claim 11 based on Brown, such claim is amended to recite forming two forms of silicon within **and filling** an opening. No new matter is added as the originally-filed application supports such amendment language at, for example, Figs. 8-13. Brown teaches partially filling an opening with amorphous silicon 61 (Figs. 2-8). In no conceivable or reasonable interpretation does such a teaching of Brown teach or suggest **filling** an opening as recited in claim 11. Therefore, Brown, or any combination of the art or record, fails to teach or suggest a positively recited limitation of claim 11, and therefore, claim 11 is allowable. Applicant respectfully requests allowance of claim 11 in the next office action.

Claims 12 and 46 depend from independent claim 11, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the anticipation rejection against claim 13 based on Brown, such claim is amended to recite forming an insulative layer over a doped region on

a semiconductor **wafer** substrate and undoped silicon being in physical contact with the doped region. No new matter is added as the originally-filed application supports such amendment language at, for example, Figs. 8-13. Brown teaches three layers of silicon form a capacitor storage node over a diffusion region 11, and one of the three layers, a doped silicon layer 41, is in contact with the diffusion region 11 in substrate 10 (col. 5, lns. 15-22; Fig. 7b). It is inconceivable that a doped silicon layer 41 in contact with a diffusion region as taught by Brown could teach or suggest an undoped silicon being in physical contact with the doped region in **a wafer** substrate as recited in claim 13. Brown, or any combination of the art of record, fails to teach or suggest a positively recited limitation of claim 13, and therefore, claim 13 is allowable. Applicant respectfully requests allowance of claim 13 in the next office action.

Claims 14-16 and 47 depend from independent claim 13, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the anticipation rejection against claim 17 based on Brown, such claim is amended to recite an undoped silicon layer and doped silicon layer together defining substantially an entirety of structural material for a capacitor storage node. No new matter is added as the originally filed application supports such limitation at, for example, Figs. 8-13. Brown teaches three layers of silicon form a capacitor storage node (Figs. 3-8). Consequently, three layers of silicon

could not teach or suggest an undoped silicon layer and doped silicon layer together defining substantially **an entirety of structural material** for a capacitor storage node as recited in claim 17. Brown, or any combination of the art of record, fails to teach or suggest a positively recited limitation of claim 17. Accordingly, claim 17 is allowable, and Applicant respectfully requests allowance of claim 17 in the next office action.

Claims 18-23 and 48 depend from independent claim 17, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the anticipation rejection against claim 24 based on Brown, such claim is amended to recite removing a portion of an insulative layer to expose a sidewall surface of a storage node comprising a first undoped silicon layer, and forming rugged polysilicon on **only** the exposed sidewall surface. No new matter is added as the originally-filed application supports such amendment language at, for example, Figs. 10-13. Brown teaches forming a HSG silicon layer from silicon layer 51 and a HSG silicon layer from silicon layer 31 (Figs. 7-8). Such a disclosure does not teach or suggest forming rugged polysilicon on **only** the exposed sidewall surface as recited in claim 24. Brown, or any combination of the art of record, fails to teach or suggest a positively recited limitation of claim 24. Accordingly, claim 24 is allowable, and Applicant respectfully requests allowance of claim 24 in the next office Action.

Claims 25 and 49 depend from independent claim 24, and therefore, are allowable for the reasons discussed above with respect to the independent claim, as well as for their own recited features which are not shown or taught by the art of record.

Regarding the rejection against claims 50-59 based on Wu, Wu is not prior art to the above-referenced application, and therefore, the rejection should be withdrawn. The priority date of the above-referenced application, July 3, 1997, proceeds the priority date of the Wu reference, January 12, 1998, and therefore, the §102(e) anticipation rejection is inappropriate. Applicant respectfully requests withdrawal of the rejection against claims 50-59 in the next office action.

A Terminal Disclaimer is provided to overcome the obviousness- type double patenting rejection against claims 50-59. Accordingly, since no other rejections are presented against claims 50-59, claims 50-59 are allowable. Applicant respectfully requests allowance of claims 50-59 in the next office action.

In view of the foregoing, allowance of all pending claims is requested. This application is now believed to be in immediate condition for allowance, and action to that end is respectfully requested. If the Examiner's next anticipated action is to be anything other than a Notice of Allowance, the undersigned respectfully requests a telephone interview prior to issuance of any such

subsequent action.

Respectfully submitted,

Dated: 3-6-03 By: _____

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application Serial No. 09/955,632
Filing Date . . . . . September 18, 2001
Inventor . . . . . Kunal R. Parekh et al.
Assignee . . . . . Micron Technology, Inc.
Group Art Unit 2813
Examiner . . . . . Y.B. Huynh
Attorney's Docket No. MI22-1816
Title: Methods of Forming Capacitors (As Amended)

VERSION WITH MARKINGS TO SHOW CHANGES MADE ACCOMPANYING RESPONSE TO NOVEMBER 6, 2002 OFFICE ACTION

The replacement specification paragraphs incorporate the following amendments. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

In the Title

On page 1, the Title has been amended as shown below:

~~Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits~~ Methods of Forming Capacitors

In the Specification

On page 1, the paragraph inserted before the "Technical Field" by the amendment dated September 18, 2001, has been amended as shown below:

CROSS REFERENCE TO RELATED APPLICATION

This patent application is a Continuation Application of U.S. Patent Application Serial No. 09/765,510, filed on January 19, 2001, now U.S. Patent No. 6,309,941, entitled "Capacitors, DRAM Arrays, Monolithic Integrated Circuits, And Methods of Forming Capacitors, DRAM Arrays, And Monolithic Integrated Circuits", naming Kunal R. Parekh, John K. Zahurak and Phillip G. Wald as inventors, which is a Continuation Application of U.S. Patent Application Serial No. 08/887,742, filed on July 3, 1997, now U.S. Patent No. 6,207,523, the disclosures of which are incorporated by reference.

In th Claims

The claims have been amended as follows. Underlines indicate insertions and ~~strikeouts~~ indicate deletions.

1. (Amended) A method of forming a capacitor comprising the following steps:

forming a capacitor plate, forming a capacitor plate comprising:

forming a solid mass of silicon material within an opening formed over a doped region of a silicon substrate, the mass comprising only two forms of silicon, the mass including undoped silicon in physical contact with the doped region; and

substantially selectively forming rugged polysilicon from one of the forms of silicon and not from another of the forms of silicon; and

forming a cell plate proximate the rugged polysilicon.

5. (Amended) A method of forming a capacitor comprising the following steps:

forming a solid mass of silicon material over a doped diffusion region of a silicon substrate, the mass comprising exposed doped silicon and exposed undoped silicon, and including undoped silicon in contact with the doped diffusion region;

substantially selectively forming rugged polysilicon from the exposed undoped silicon and not from the exposed doped silicon; and

forming a cell plate proximate the rugged polysilicon.

11. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region of a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming two forms of silicon within and filling the opening, the two forms of silicon including undoped silicon in contact with the doped region;

exposing the two forms of silicon to common subsequent processing conditions which substantially selectively form rugged polysilicon from one of the exposed two forms of silicon and not from another of the exposed two forms of silicon; and

forming a cell plate proximate the ~~storage node~~ rugged polysilicon.

13. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor wafer substrate;

forming an opening through the insulative layer to the doped region;

forming silicon material within the opening, the silicon material comprising doped silicon and undoped silicon and defining a capacitor storage node, a portion of the undoped silicon being in physical contact with the doped region;

removing a portion of the insulative layer to expose a sidewall surface of the storage node, the exposed sidewall surface comprising undoped silicon;

forming HSG from the undoped silicon of the exposed sidewall surface; and

forming a cell plate proximate the storage node.

17. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming an undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon contacting the doped region;

forming a doped silicon layer within the narrowed opening, the undoped silicon layer and doped silicon layer together defining substantially an entirety of structural material for a capacitor storage node; and

forming a cell plate proximate the storage node.

24. (Amended) A method of forming a capacitor comprising the following steps:

forming an insulative layer over a doped region on a semiconductor substrate;

forming an opening through the insulative layer to the doped region;

forming a first undoped silicon layer within the opening to narrow the opening, a portion of the undoped silicon layer contacting the doped region;

forming a doped silicon layer within the narrowed opening to further narrow the opening;

forming a second undoped silicon layer within the further narrowed opening; the first undoped silicon layer, second undoped silicon layer and doped silicon layer together defining a capacitor storage node;

removing a portion of the insulative layer to expose a sidewall surface of the storage node comprising the first undoped silicon layer;

forming rugged polysilicon on only the exposed sidewall surface; and

forming a cell plate proximate the storage node.

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